UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,922,082 B2
APPLICATION NO. : 10/676345
DATED : July 26, 2005
INVENTOR(S) : Wijeratne

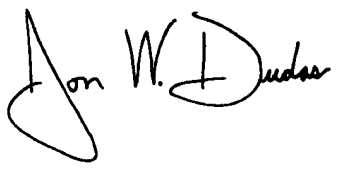
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Drawings:
Fig. 1, "LVS MUX 10" should read --LVS CIRCUIT 10--;
Fig. 2, "LVS MUX 20" should read --LVS CIRCUIT 20--;
Fig. 2, "BUFFERS" should read --BUFFERING INVERTERS--;
Fig. 3, "n1" should read --N1--;
Fig. 3, "n2" should read --N2--;
Fig. 3, "n3" should read --N3--;
Fig. 3, "p1" should read --P1--;
Fig. 3, "p2" should read --P2--;
Fig. 3, "INPUT/OUTPUT DEVICE 142" should read --INPUT/OUTPUT MODULE 142--;

In the Claims:
Col. 3, line 35, "...signals LCS-IN1, LCS-IN2, and LCS-IN3 respectively..." should read --...signals LVS-IN1, LVS-IN2, and LVS-IN3 respectively...--;
Col. 6, line 51, "...signal 90 provides..." should read --...signal 94 provides...--;
Col. 8, line 4, "...the inverters 46, are..." should read --... the buffering inverters 52, are...--;
Col. 9, line 52, "...the LVS circuit 12." should read --...the LVS circuit 10.--;
Col. 9, line 67, "...art select logic circuit 10..." should read --...art LVS circuit 10...--;
Col. 10, line 34, "...memory 146 include..." should read --...memory 136 include...--; and
Col. 13, line 7, "...a central processor unit..." should read --...a central processing unit...--.

Signed and Sealed this

Fifth Day of February, 2008



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